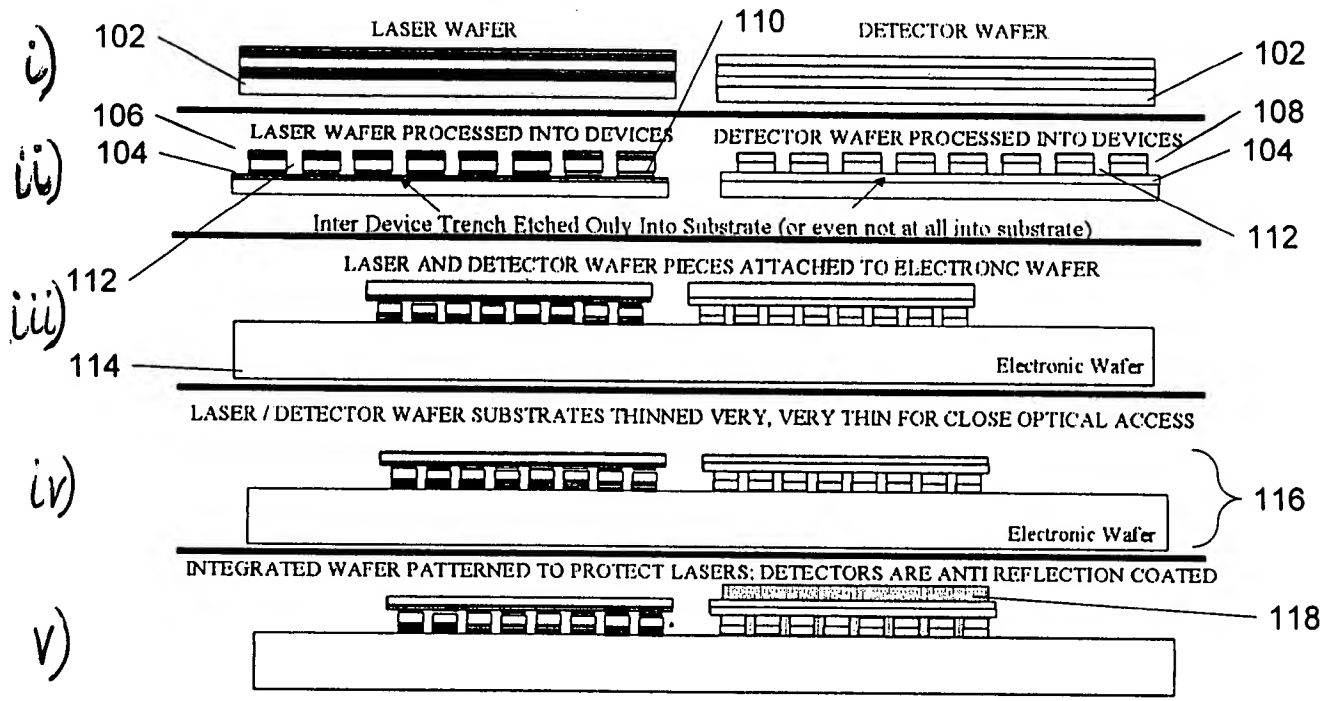


FIG. 1

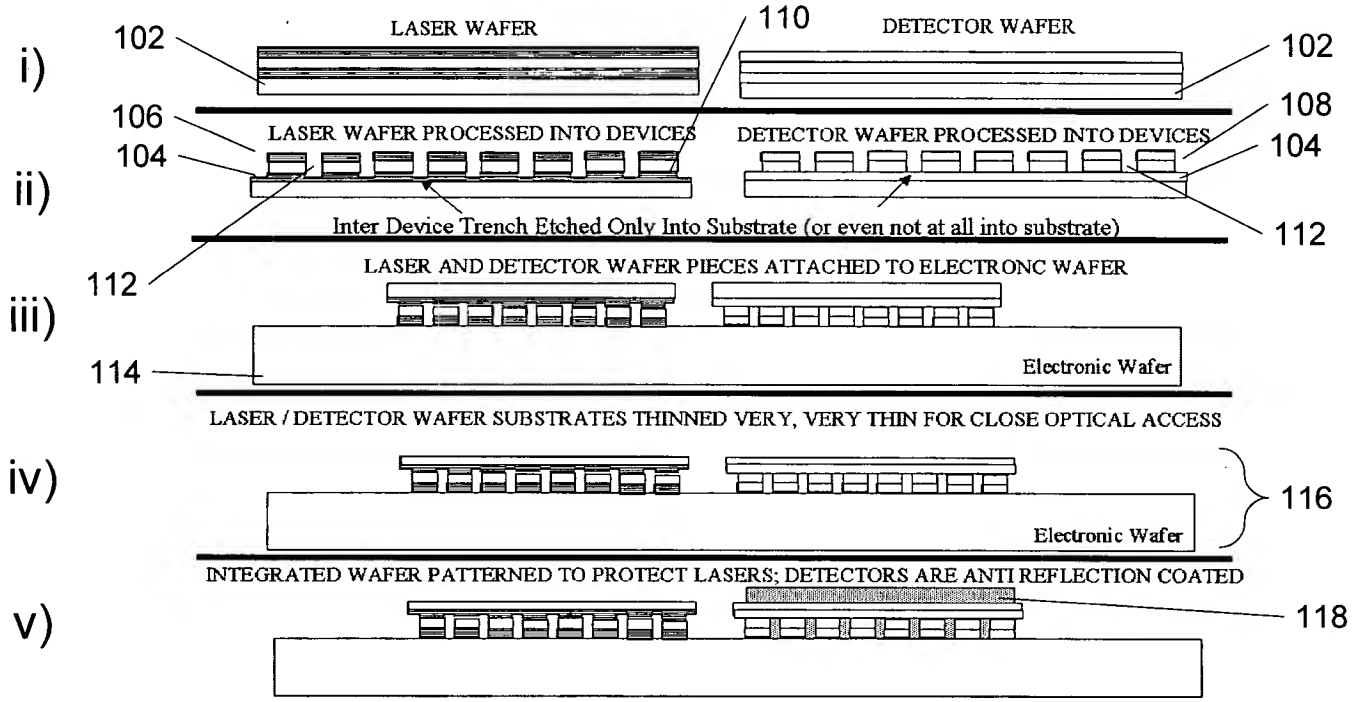


FIG. 1

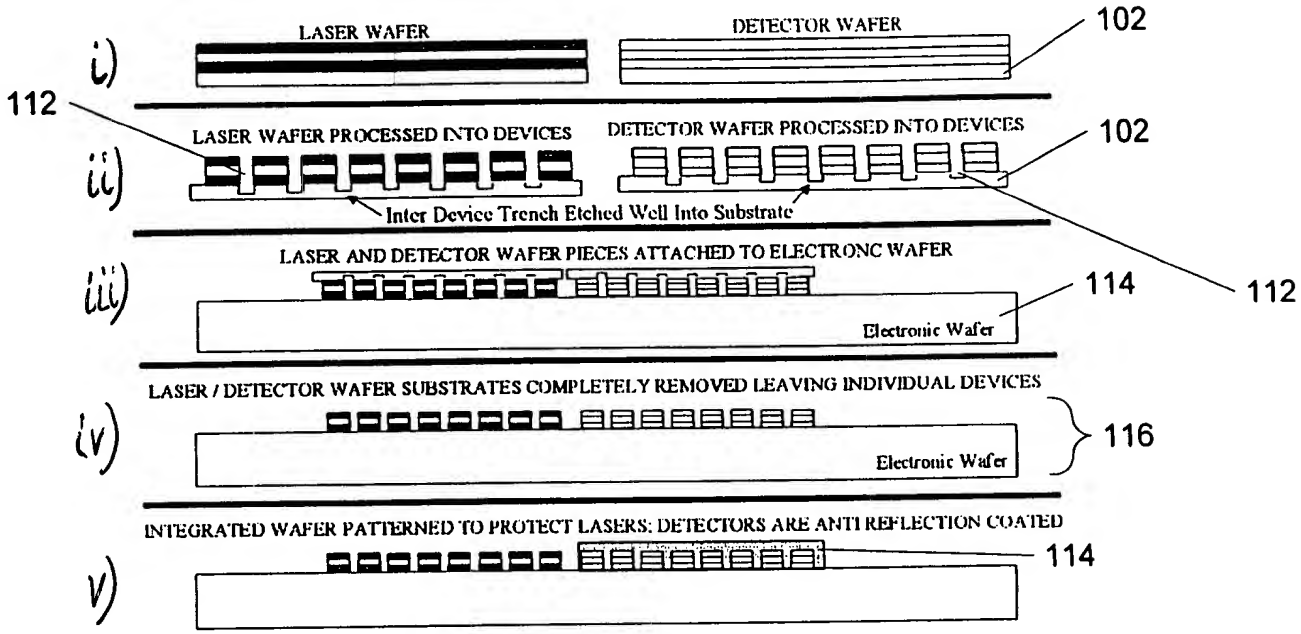


FIG. 2

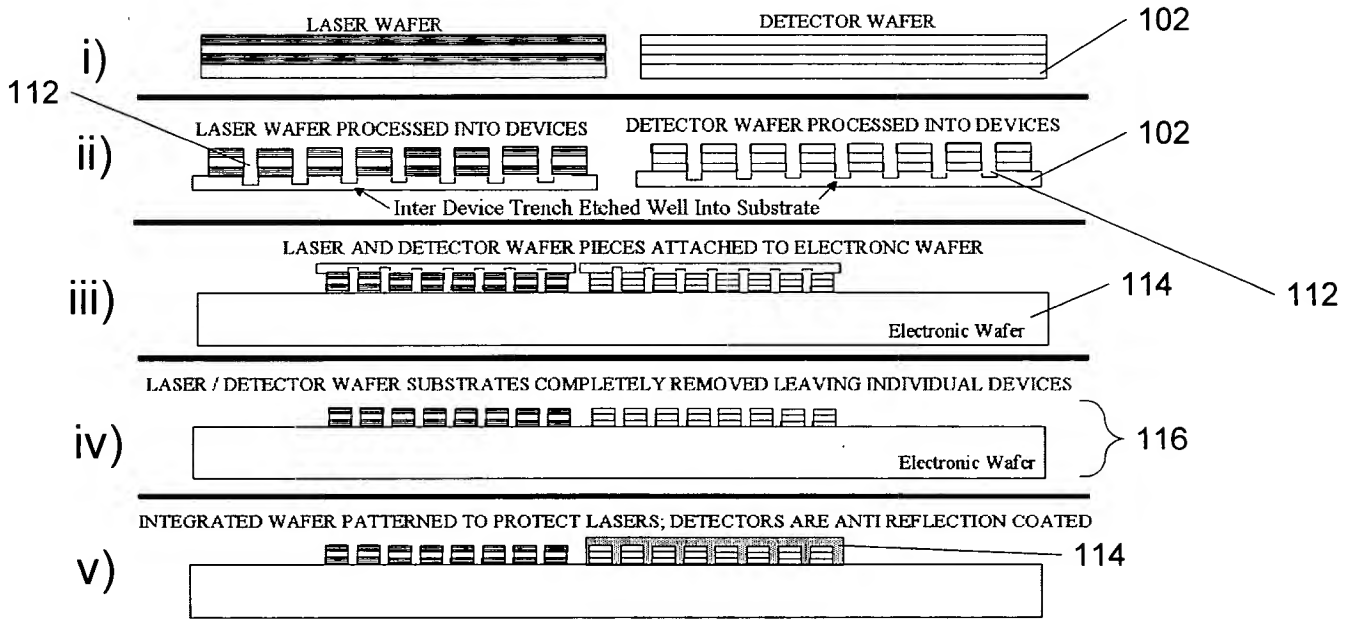


FIG. 2

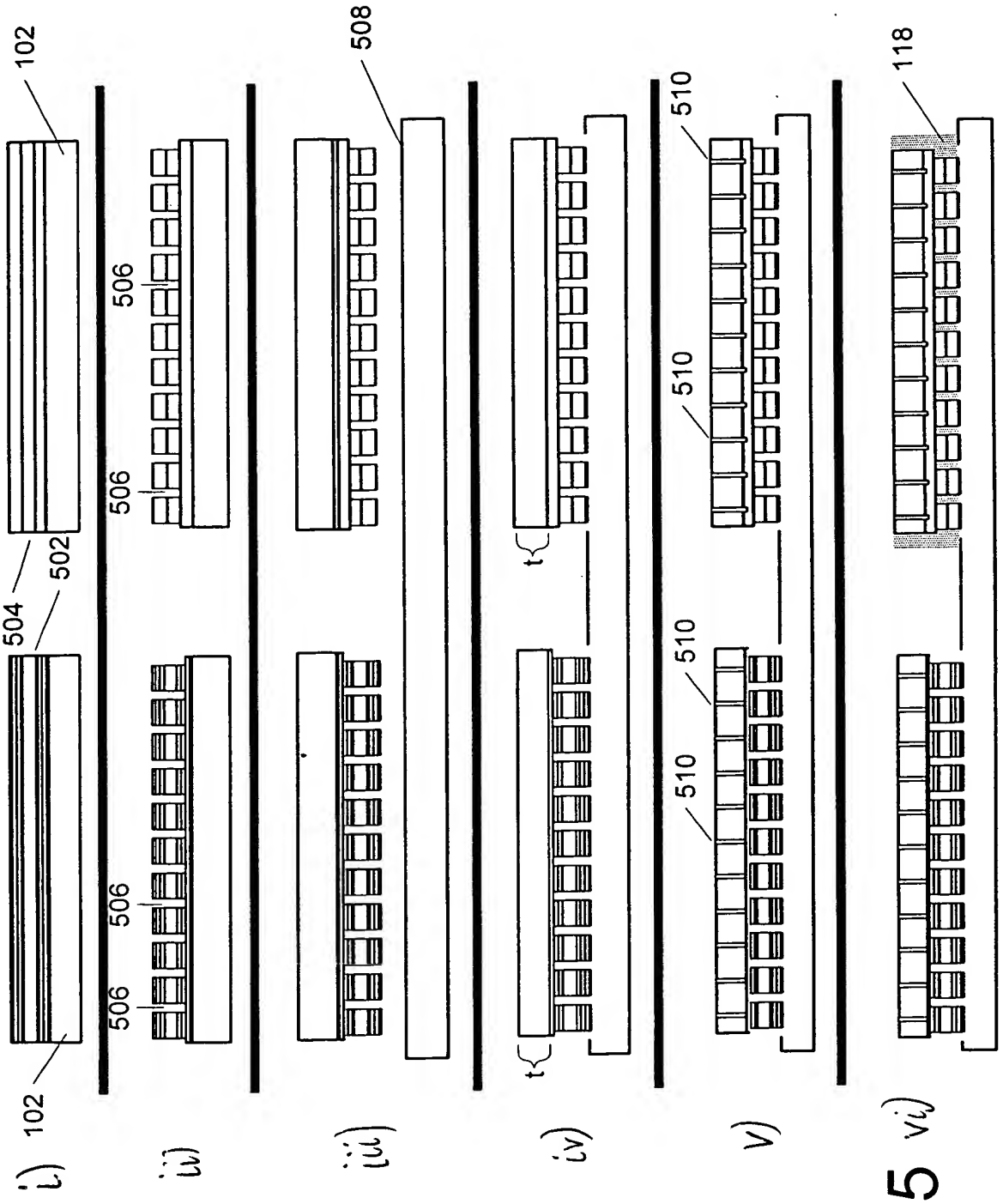


FIG. 5

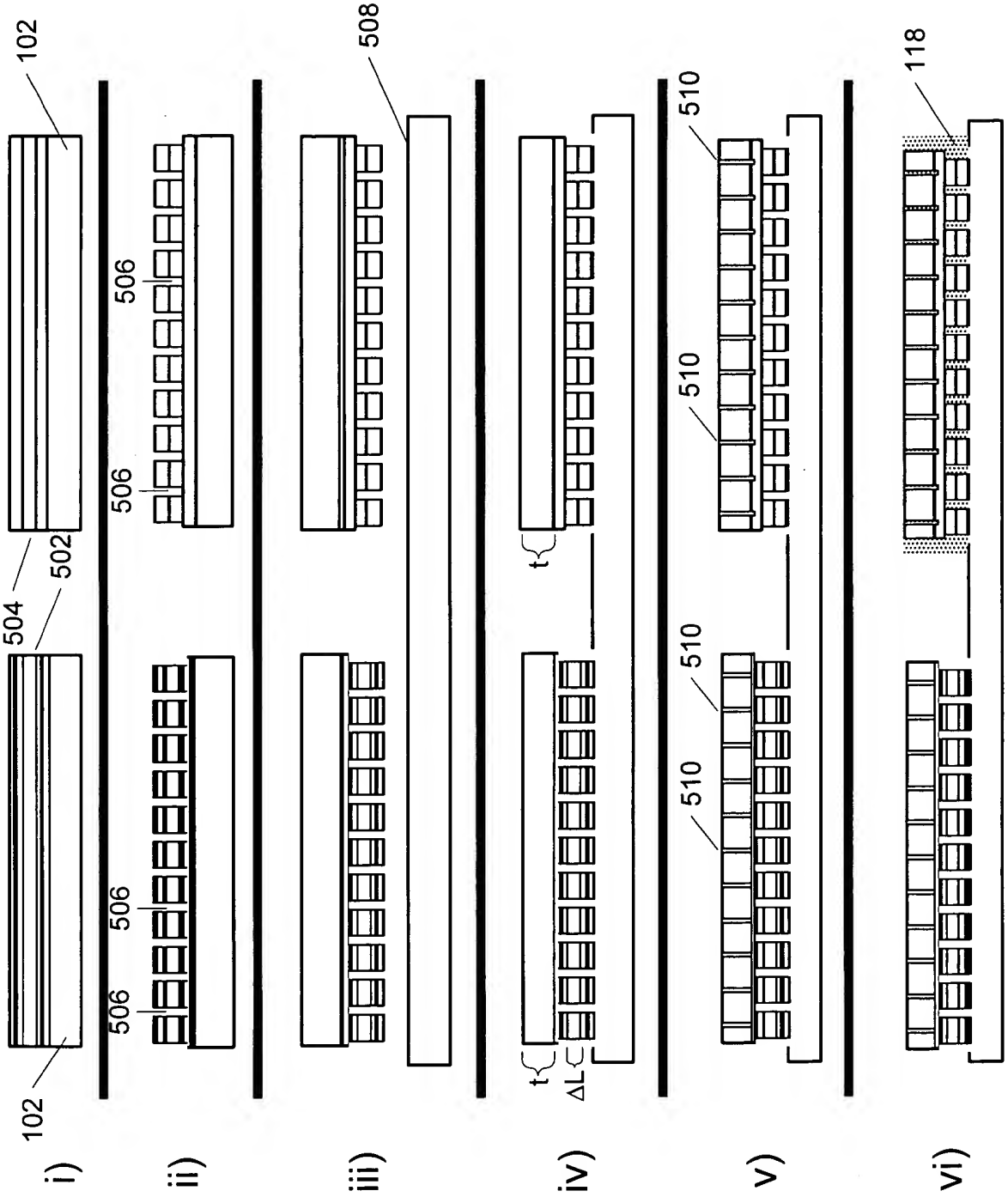


FIG. 5

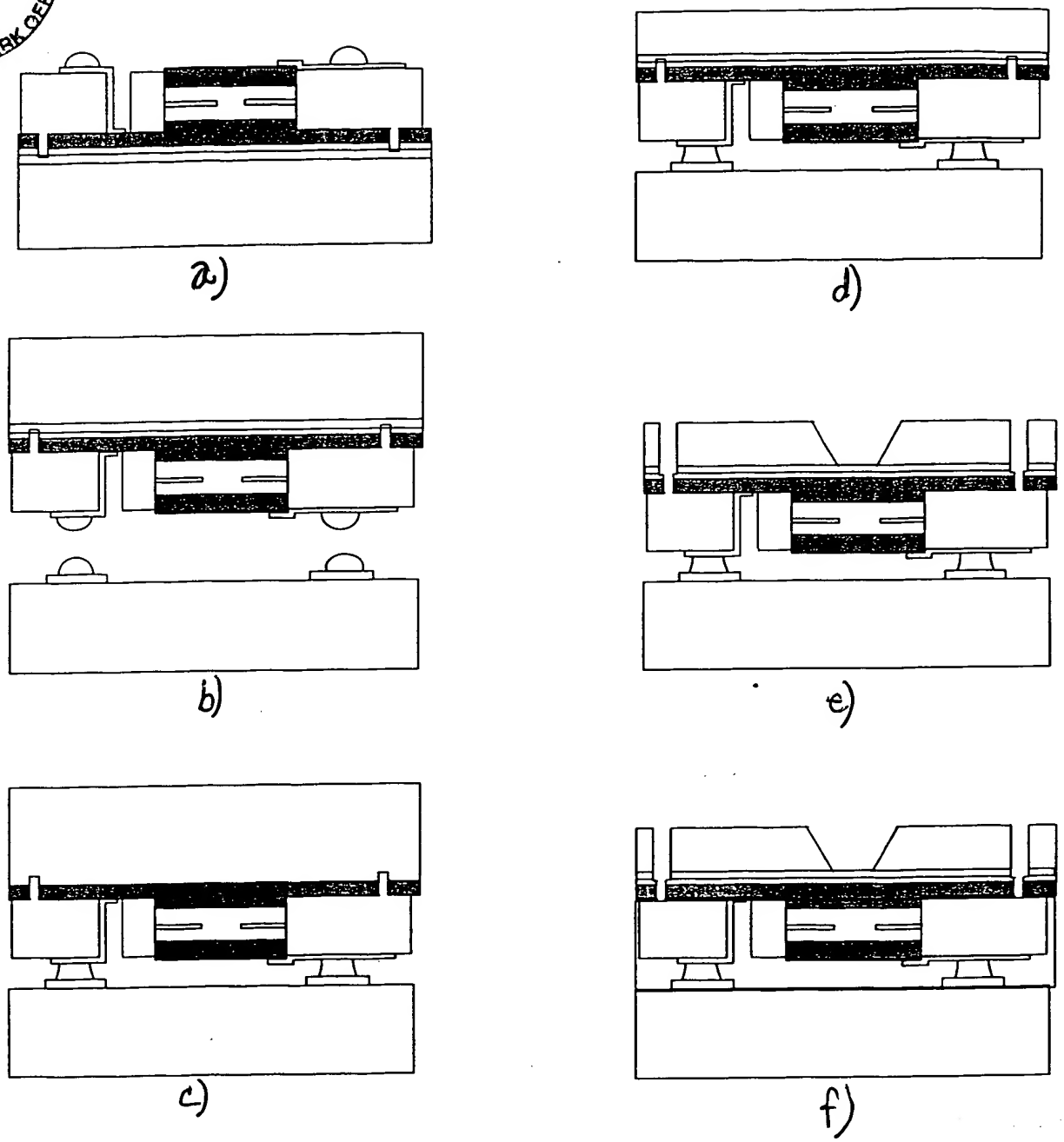
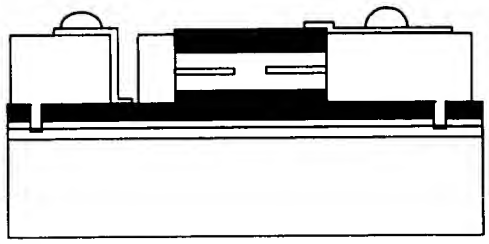
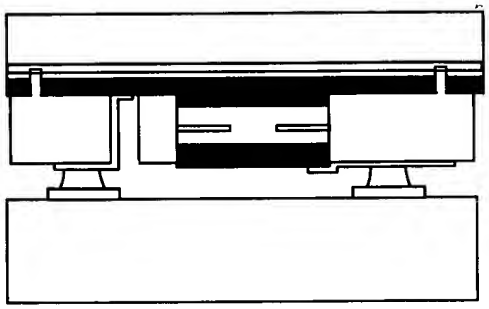


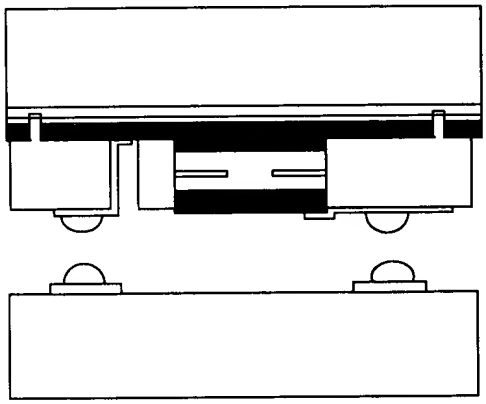
FIG. 12



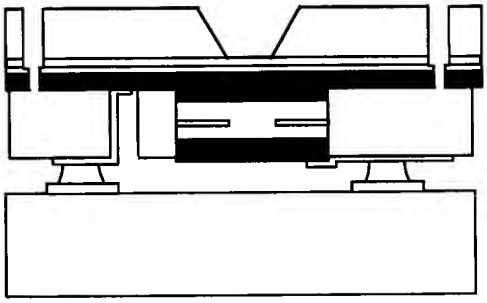
a)



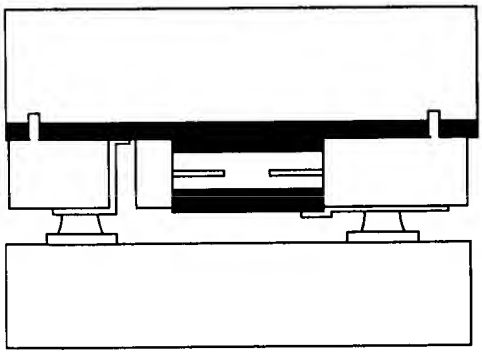
d)



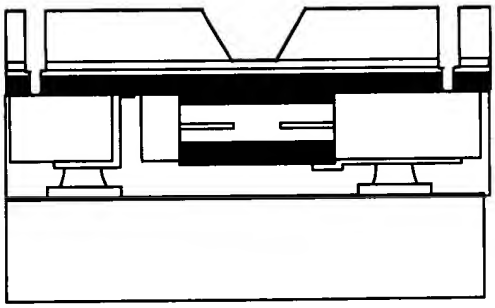
b)



e)



c)



f)

FIG. 12

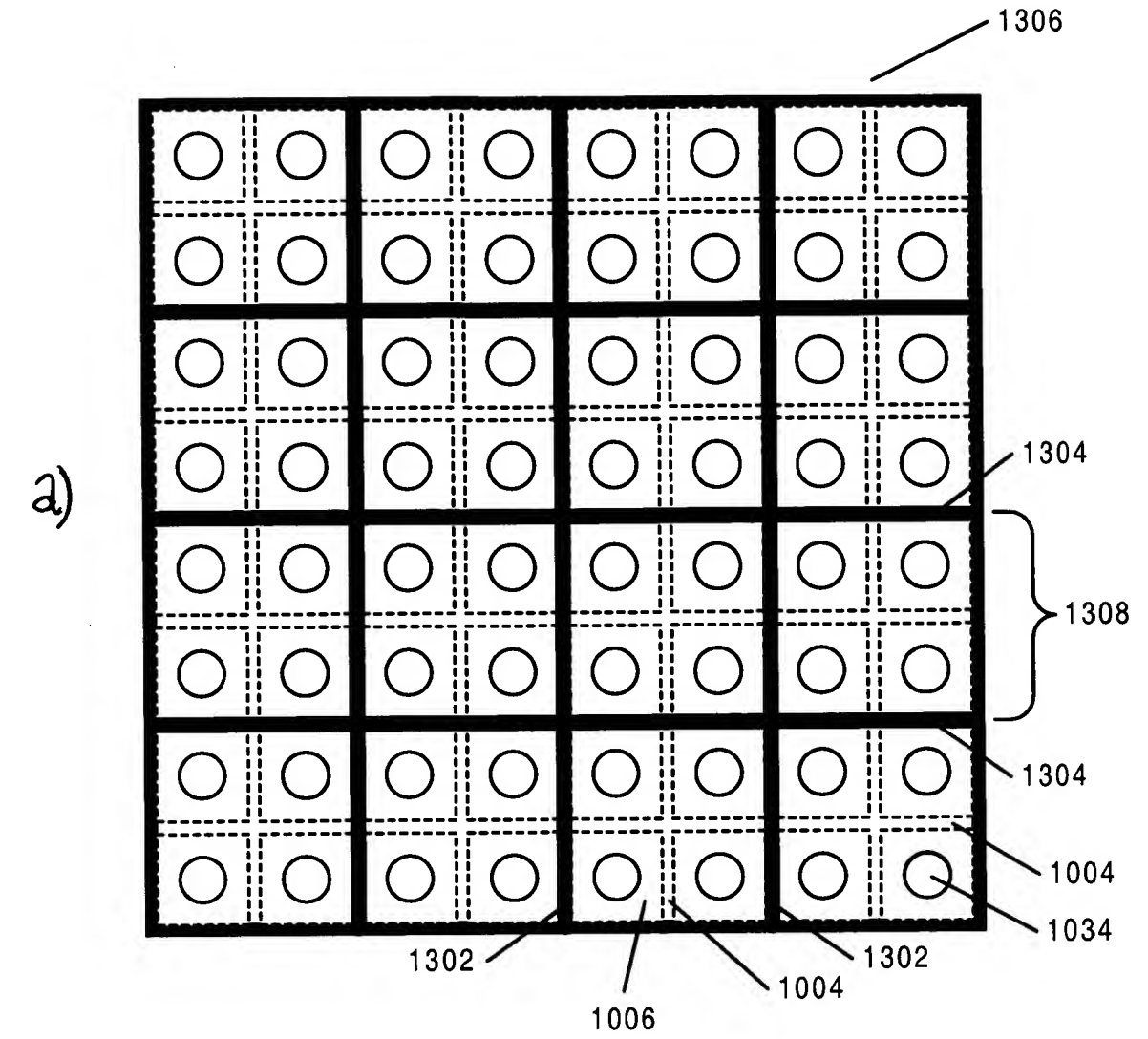


FIG. 13

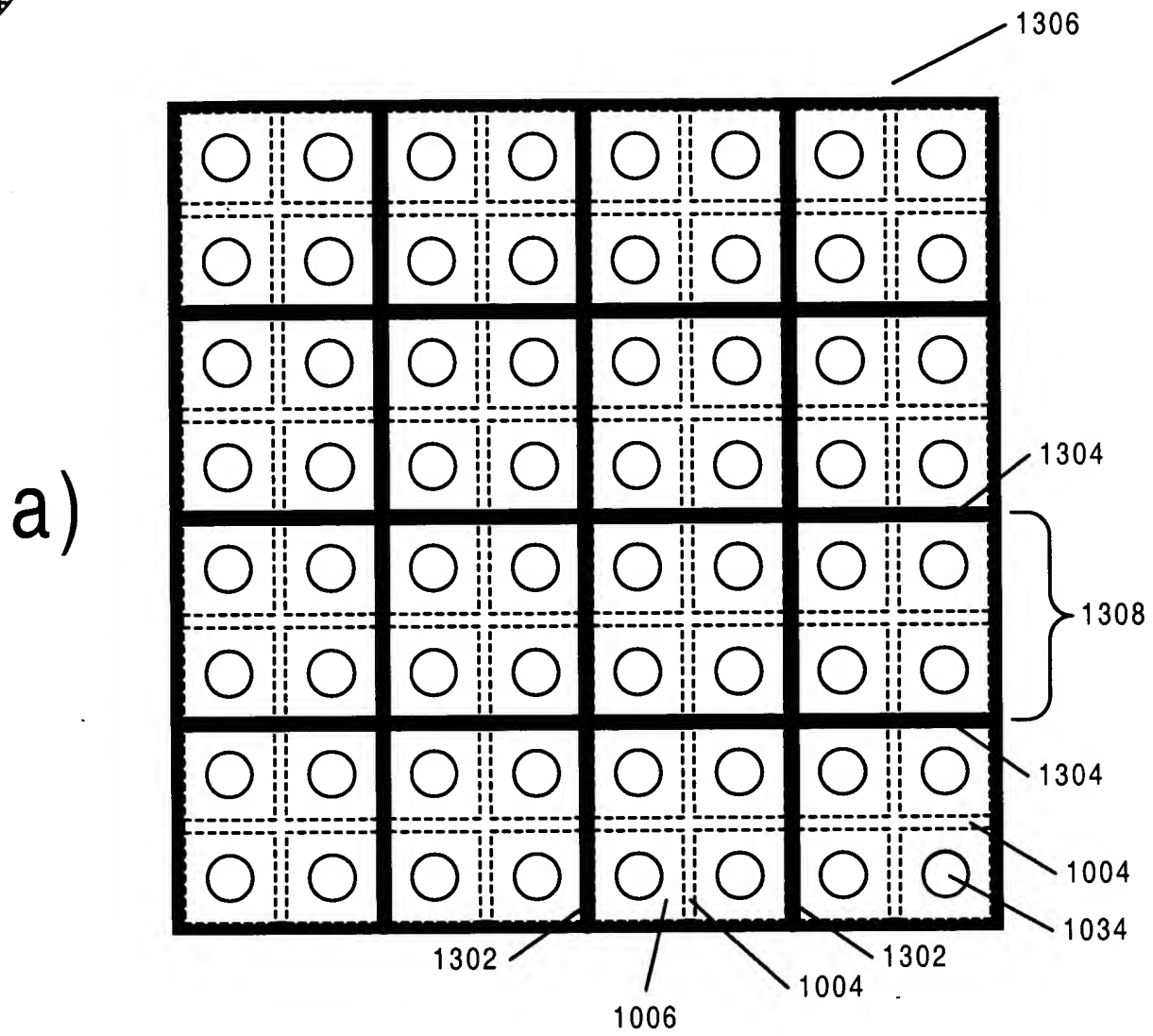


FIG. 13

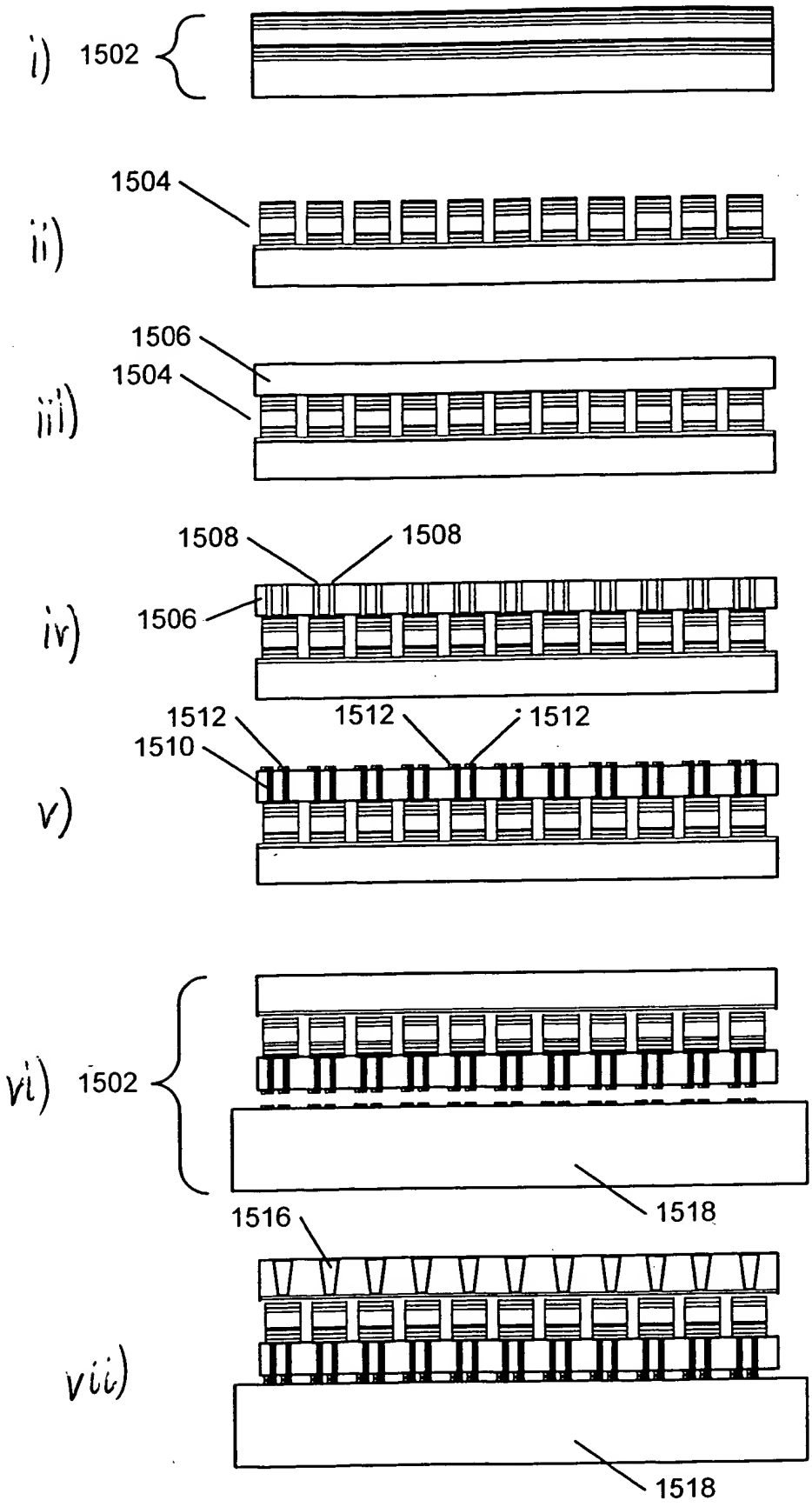


FIG. 15

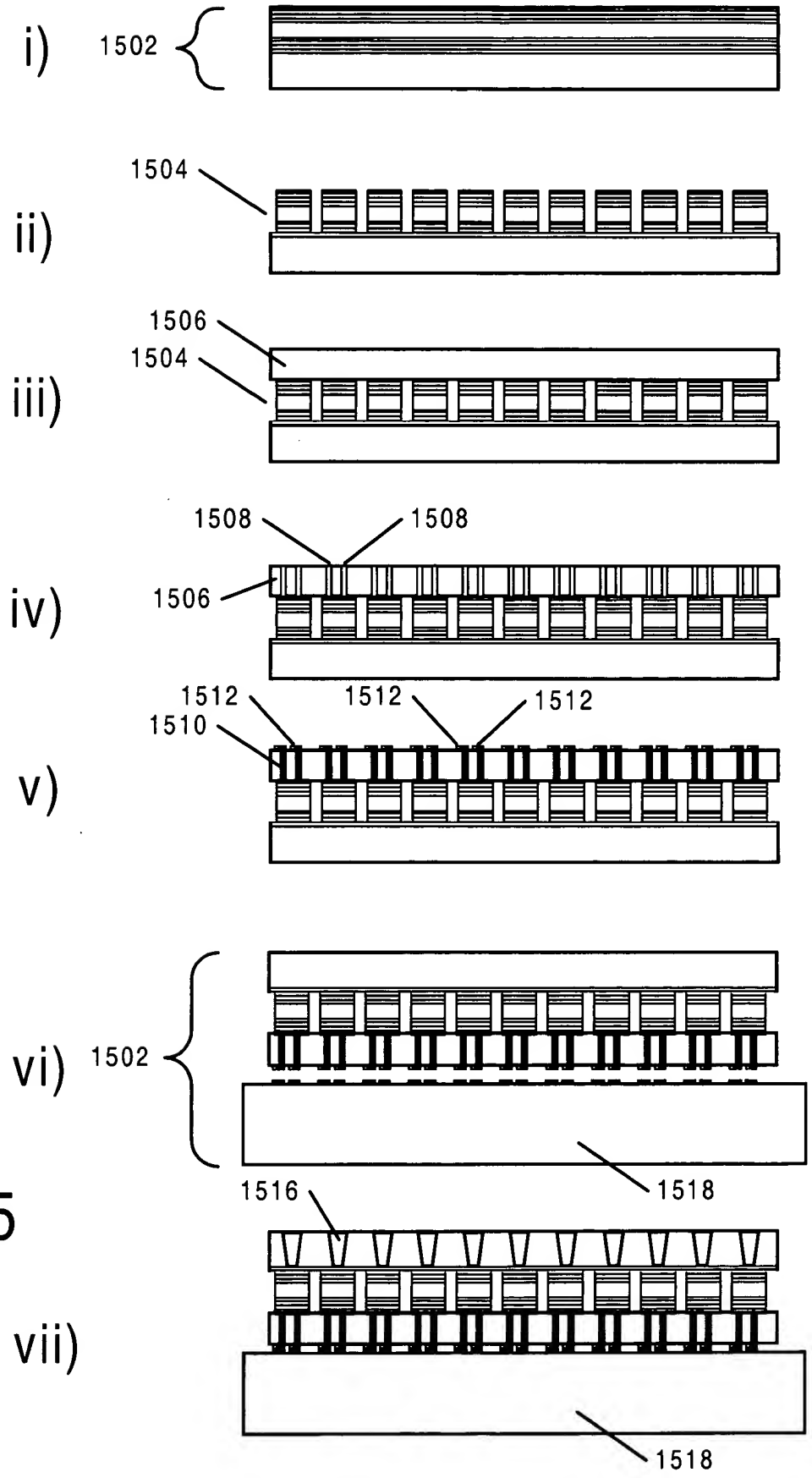


FIG. 15

i) Optical wafers (e.g Laser and Detector wafers)

ii) Process into individual devices

iii) (Optional) Attach carrier

iv) Thin substrate to appropriate thickness to facilitate etching

v) Etch vias (or drill holes) and pattern with insulator

vi) Fill vias or holes with conductive material

vii) Pattern wafer substrate to match pad locations on electronic chip

viii) Attach optical chip to electronic chip using now matching pad locations

ix) (Optional) Remove holder

(Optional) AR coat detectors

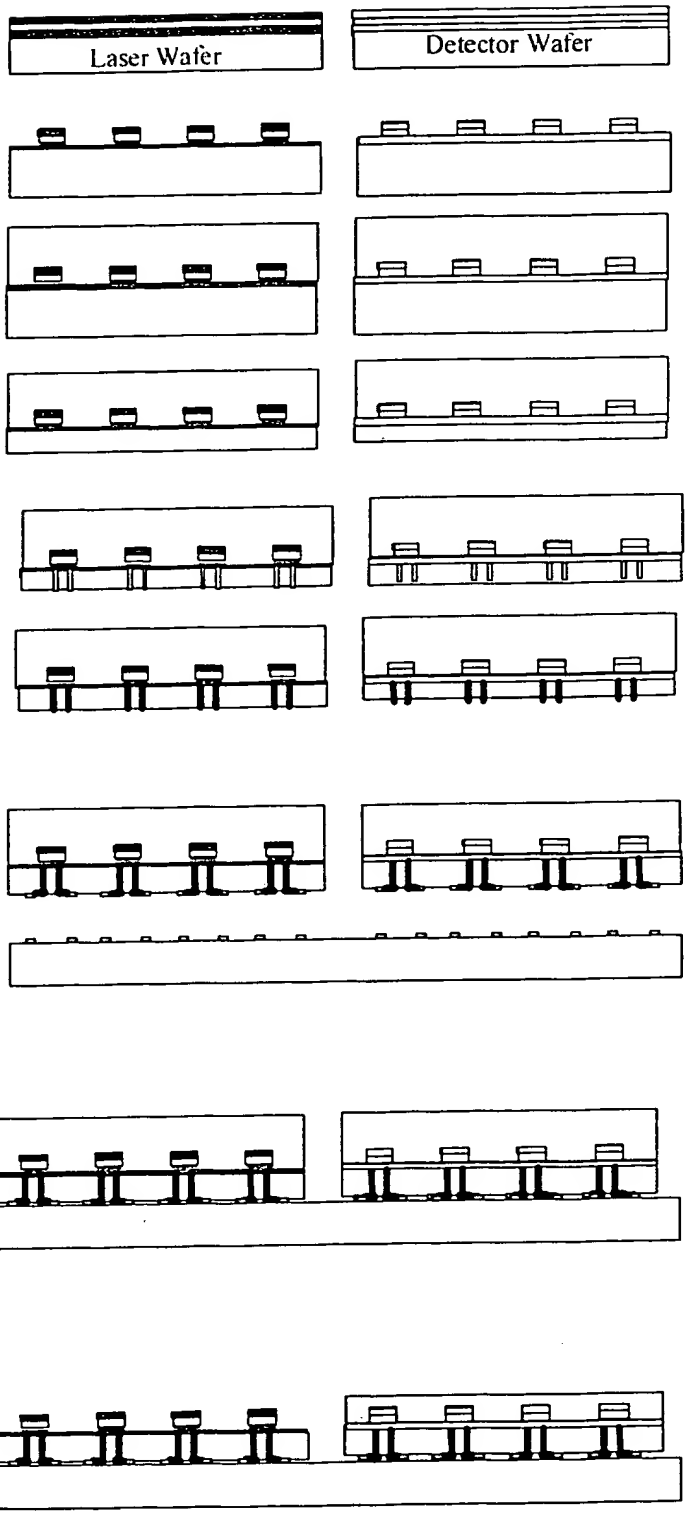


FIG. 16A

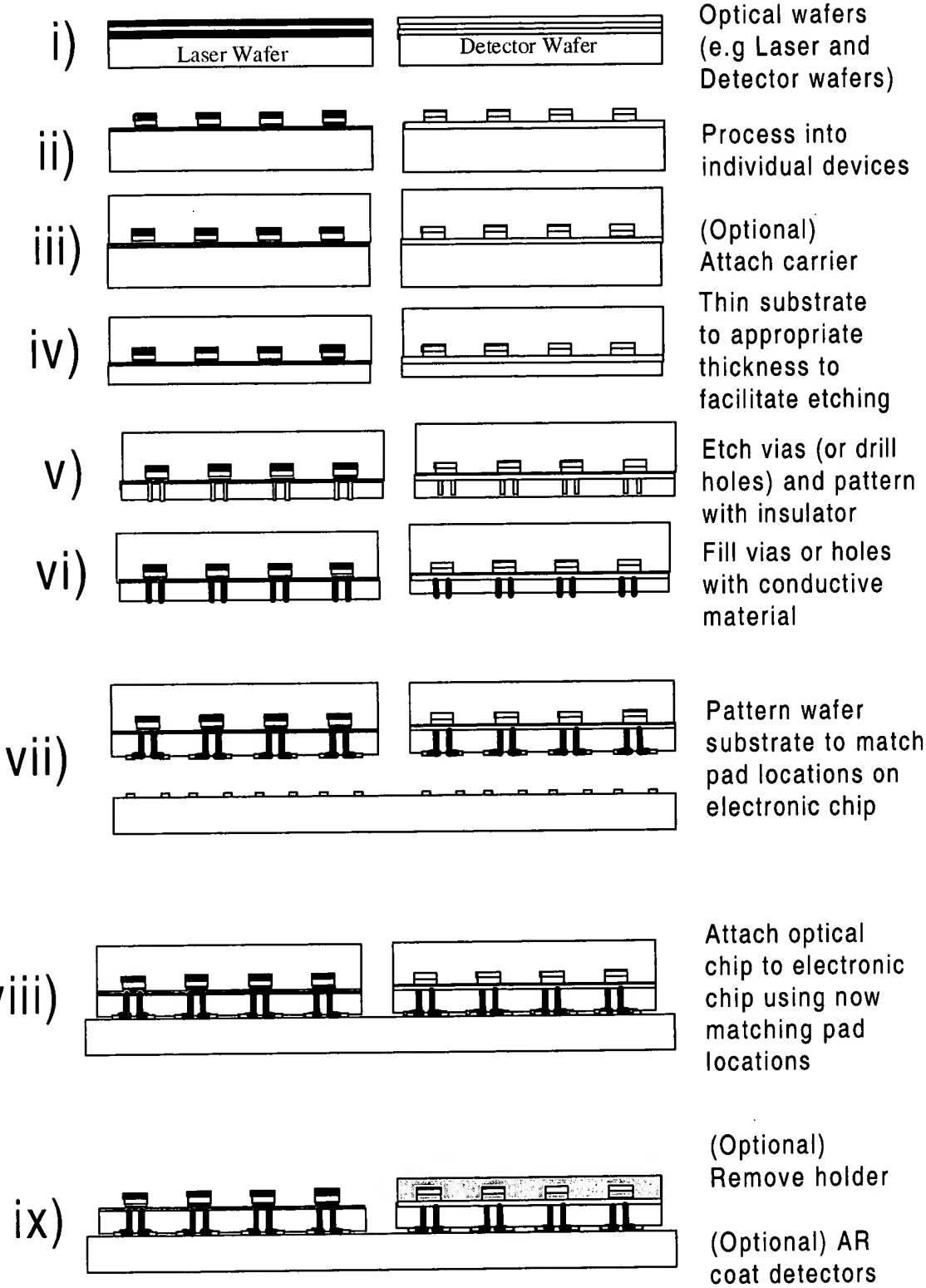


FIG. 16A

FIG. 16B

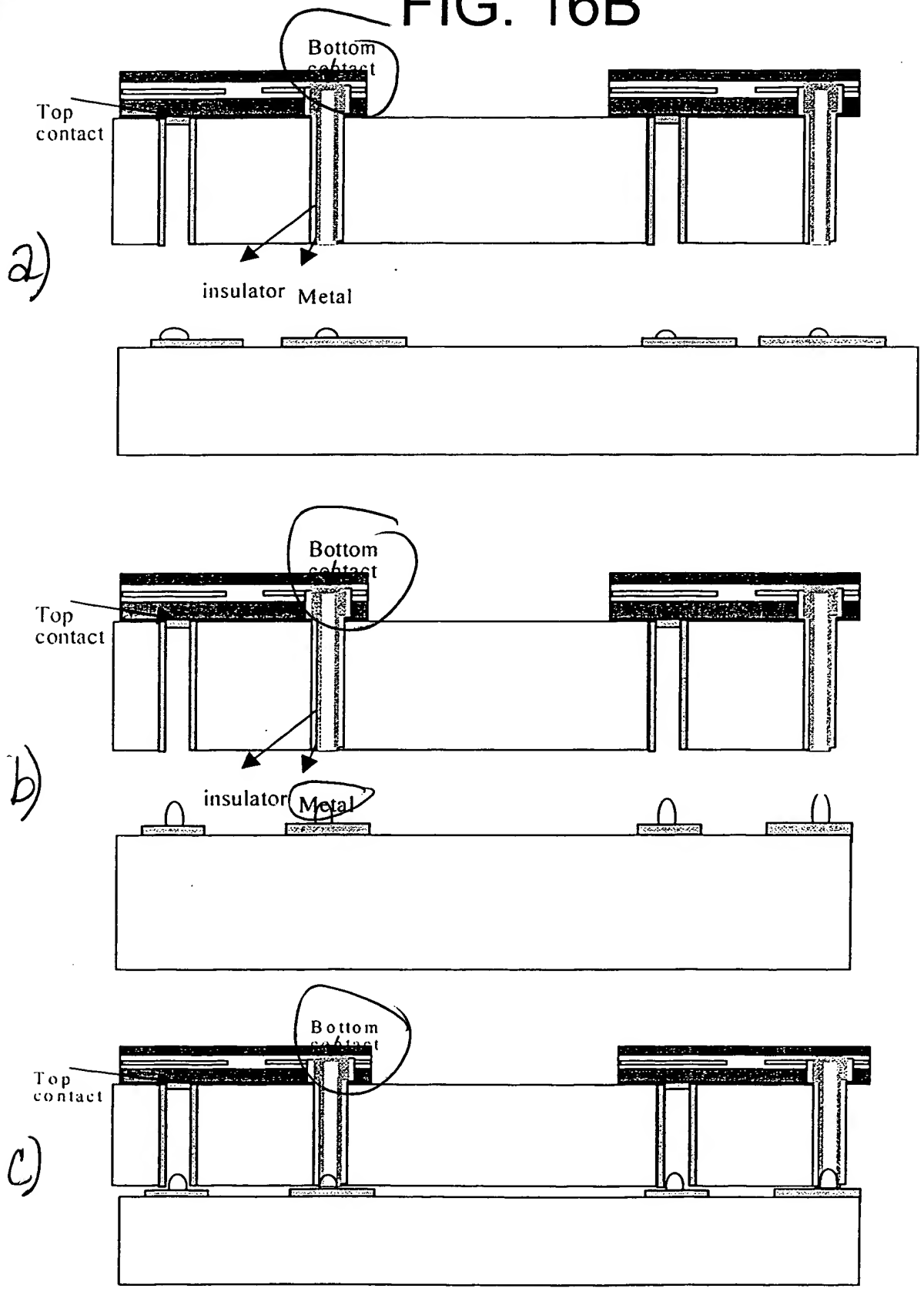


FIG. 16B

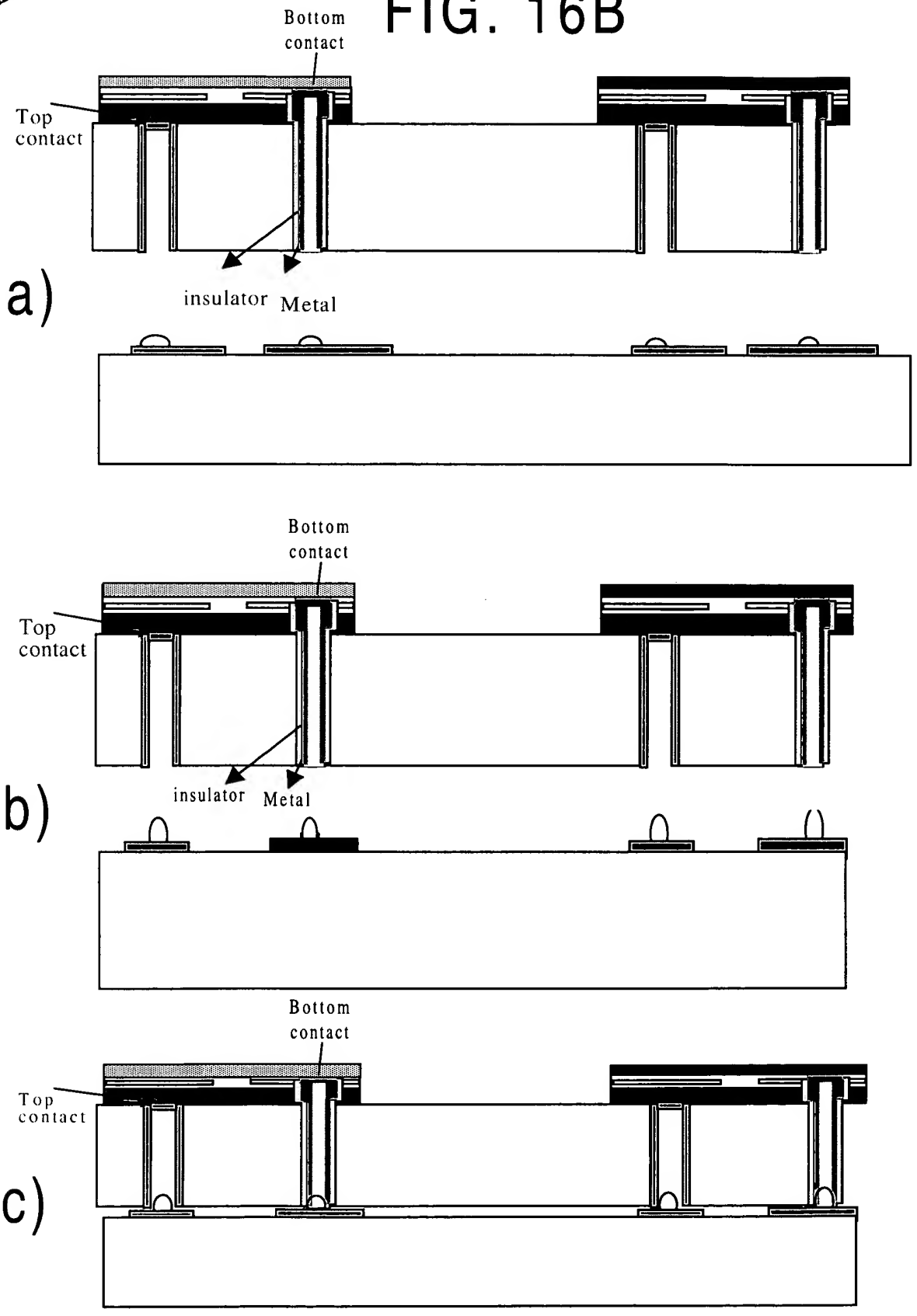


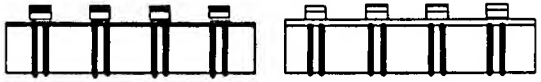
FIG. 17

i) Optical wafers (e.g. Laser & Detector Wafers)

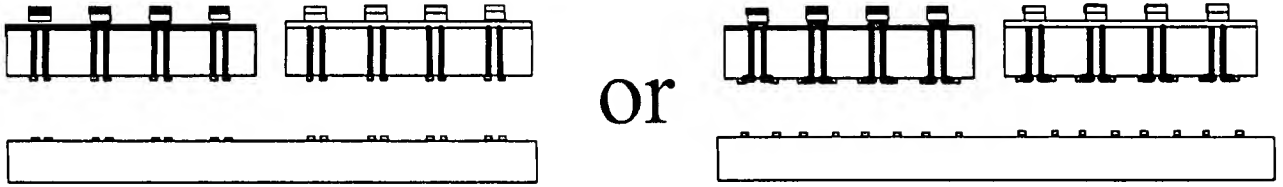
ii) Process wafers into discrete devices

iii) Etch vias or holes & Pattern with insulator

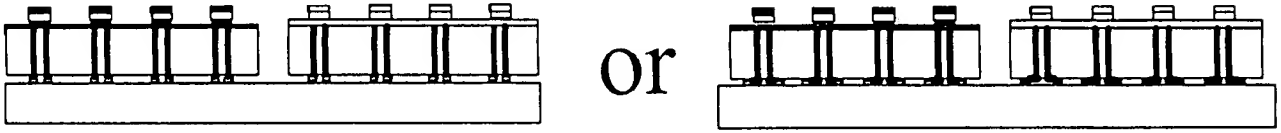
iv) Fill with conductor to backside



v) Pattern wafer backside to match pad locations on electronic wafer



vi) Attach optics to electronic wafer pad locations



vii) AR Coat Detectors (optional)

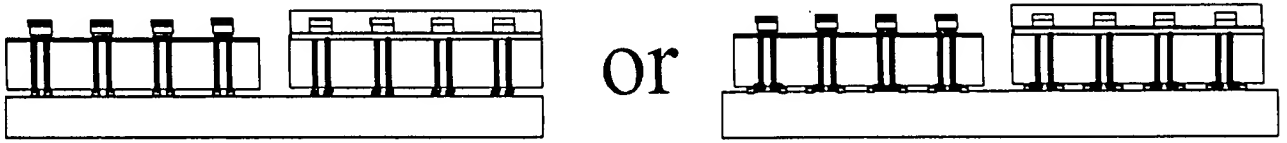
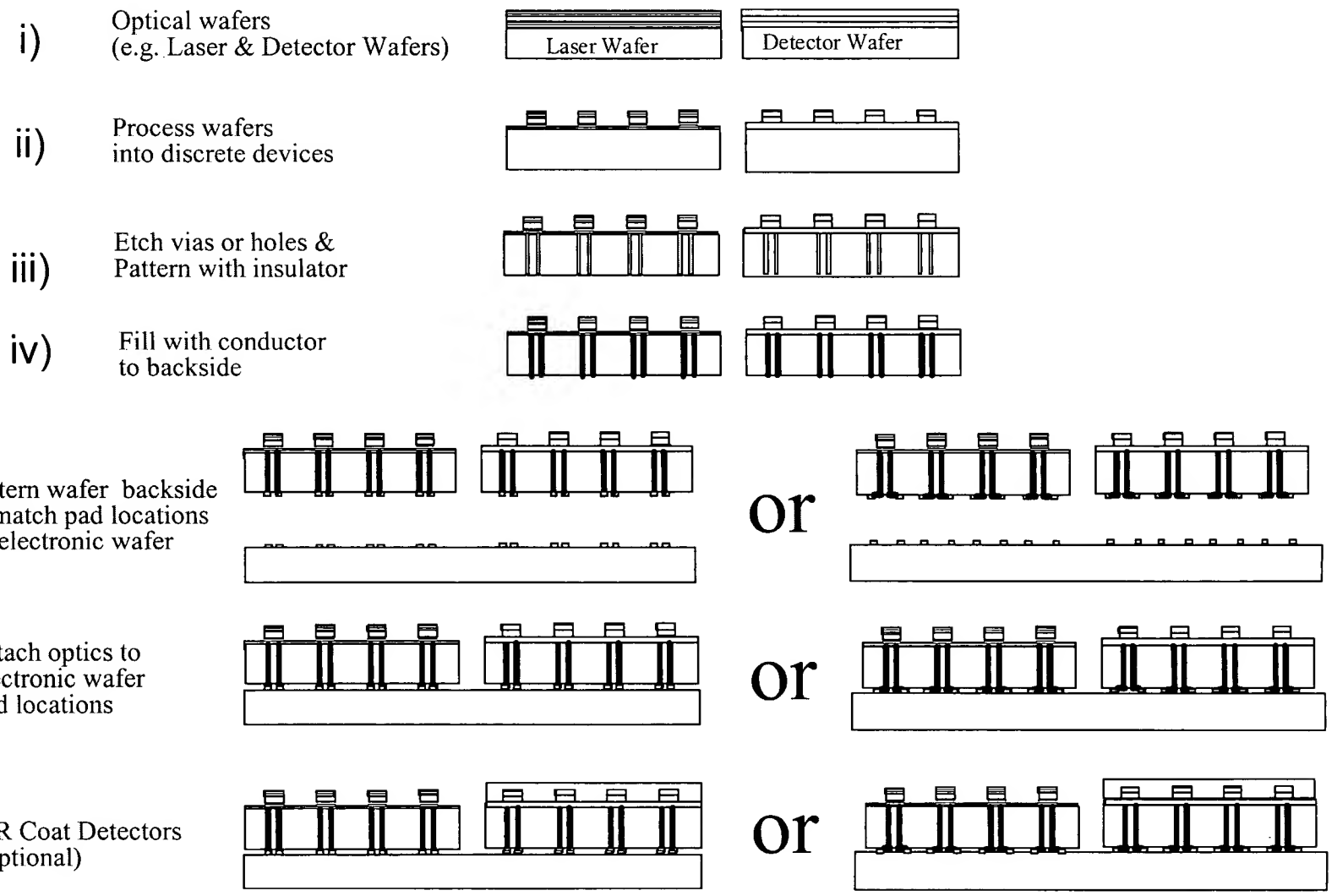


FIG. 17



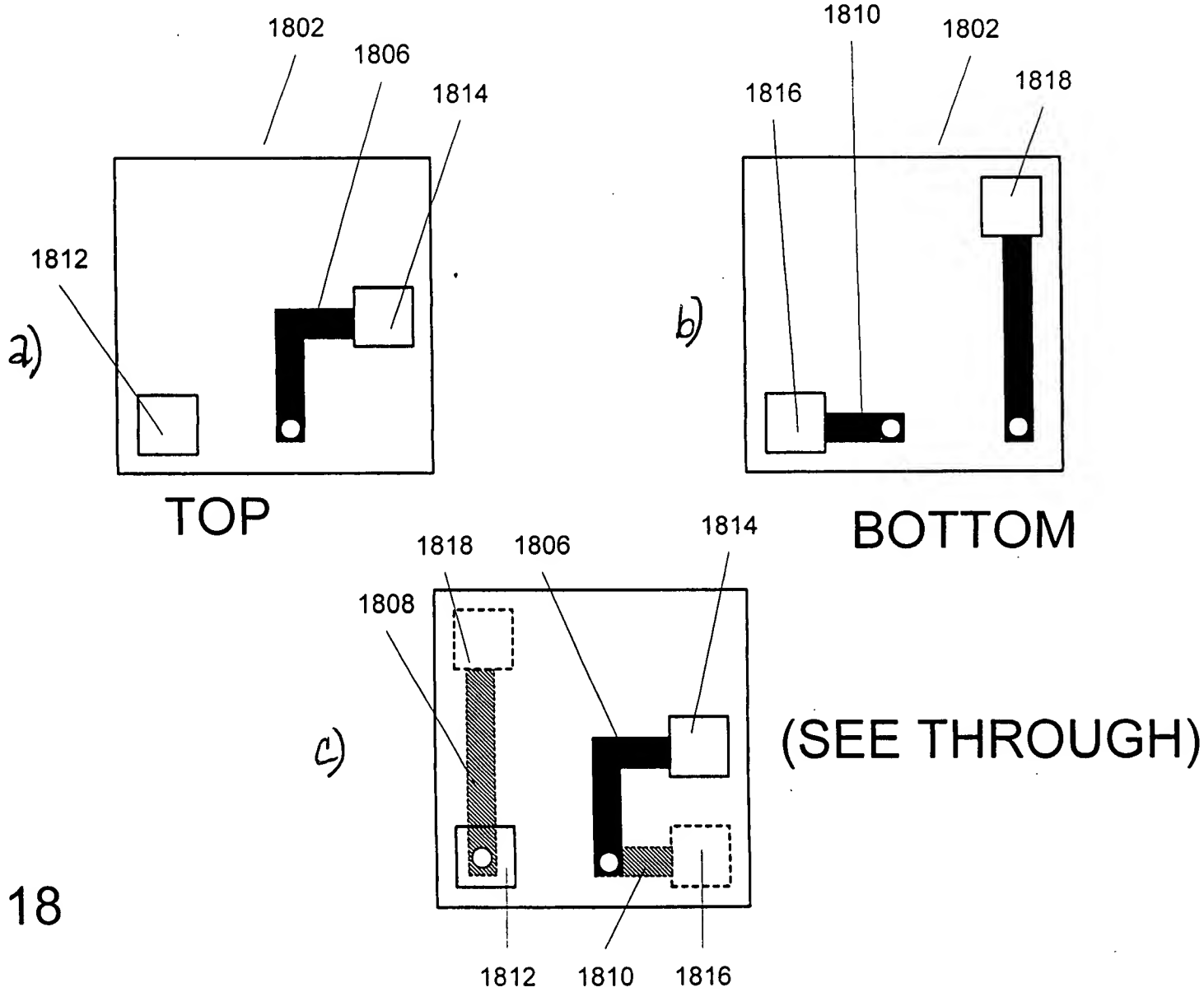


FIG. 18

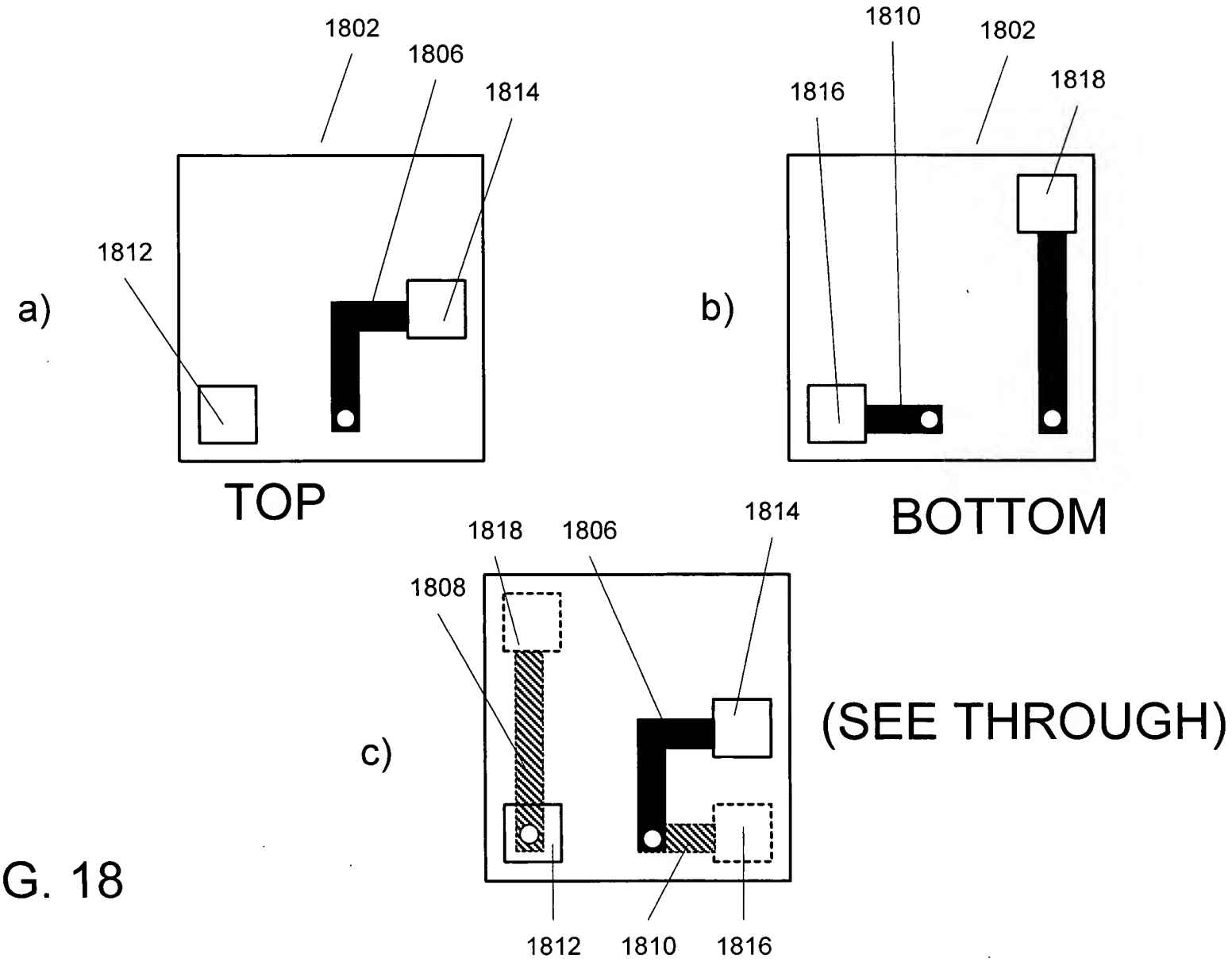
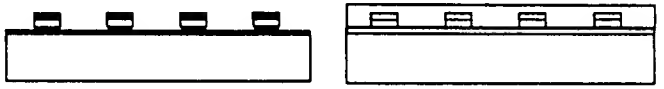


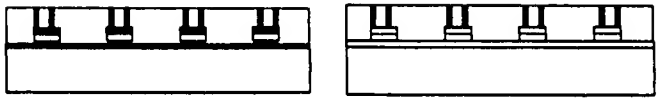
FIG. 18

i) Optical wafers
(e.g Laser & Detector wafers)

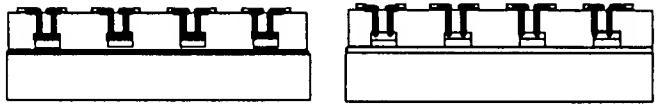
ii) Process into individual devices
& AR coat detectors



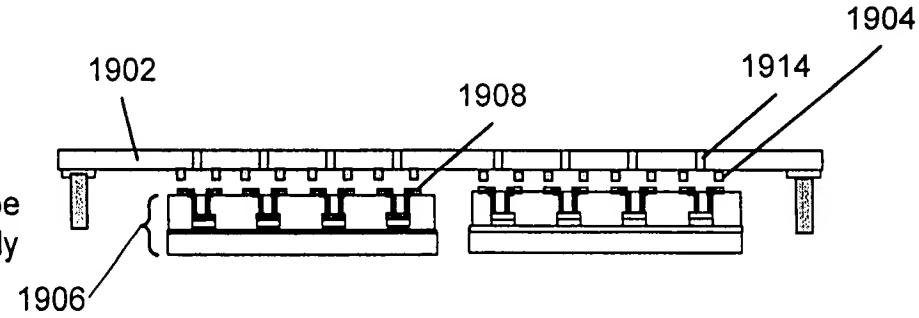
iii) Cover devices with insulator and
pattern vias through to device
contact pads



iv) Pattern optical device wafer
to create traces to locations
that will match mating
contacts on adapter



v) Attach optical device chip
to adapter via aligning
pads created by patterning
(NOTE: Holes in adapter can be
created pre-post or concurrently
with wafer patterning



vi) Integrate adapter chip with
electronic chip via standoffs,
wires, etc.

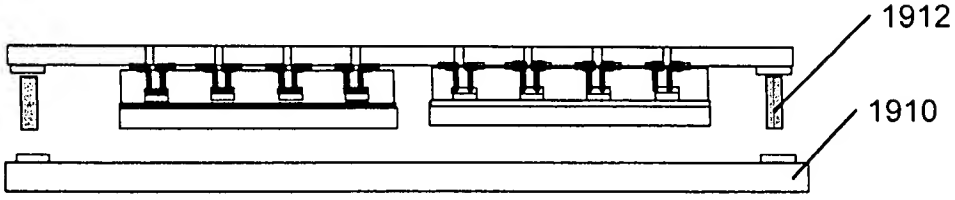


FIG. 19

i) Optical wafers (e.g Laser & Detector wafers)

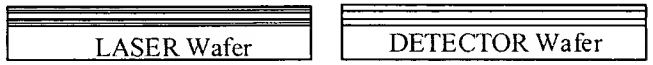
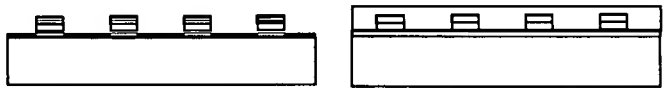
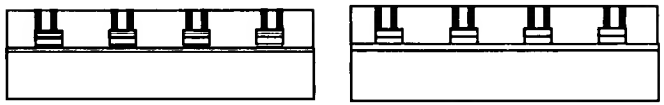


FIG. 19

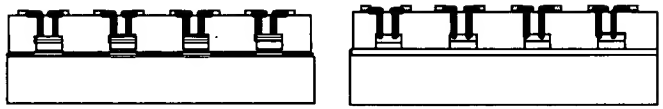
ii) Process into individual devices & AR coat detectors



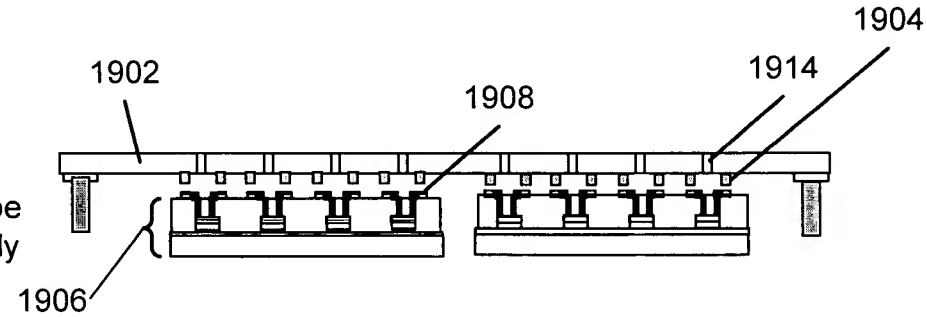
iii) Cover devices with insulator and pattern vias through to device contact pads



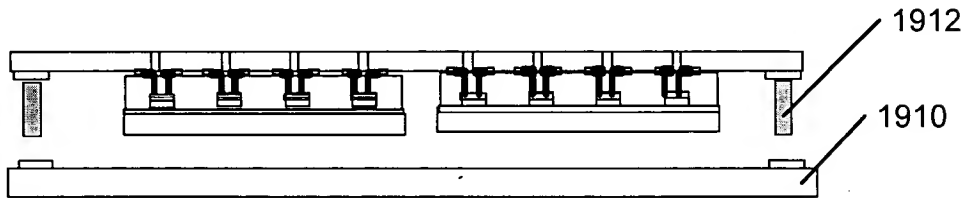
iv) Pattern optical device wafer to create traces to locations that will match mating contacts on adapter



v) Attach optical device chip to adapter via aligning pads created by patterning (NOTE: Holes in adapter can be created pre-post or concurrently with wafer patterning



vi) Integrate adapter chip with electronic chip via standoffs, wires, etc.



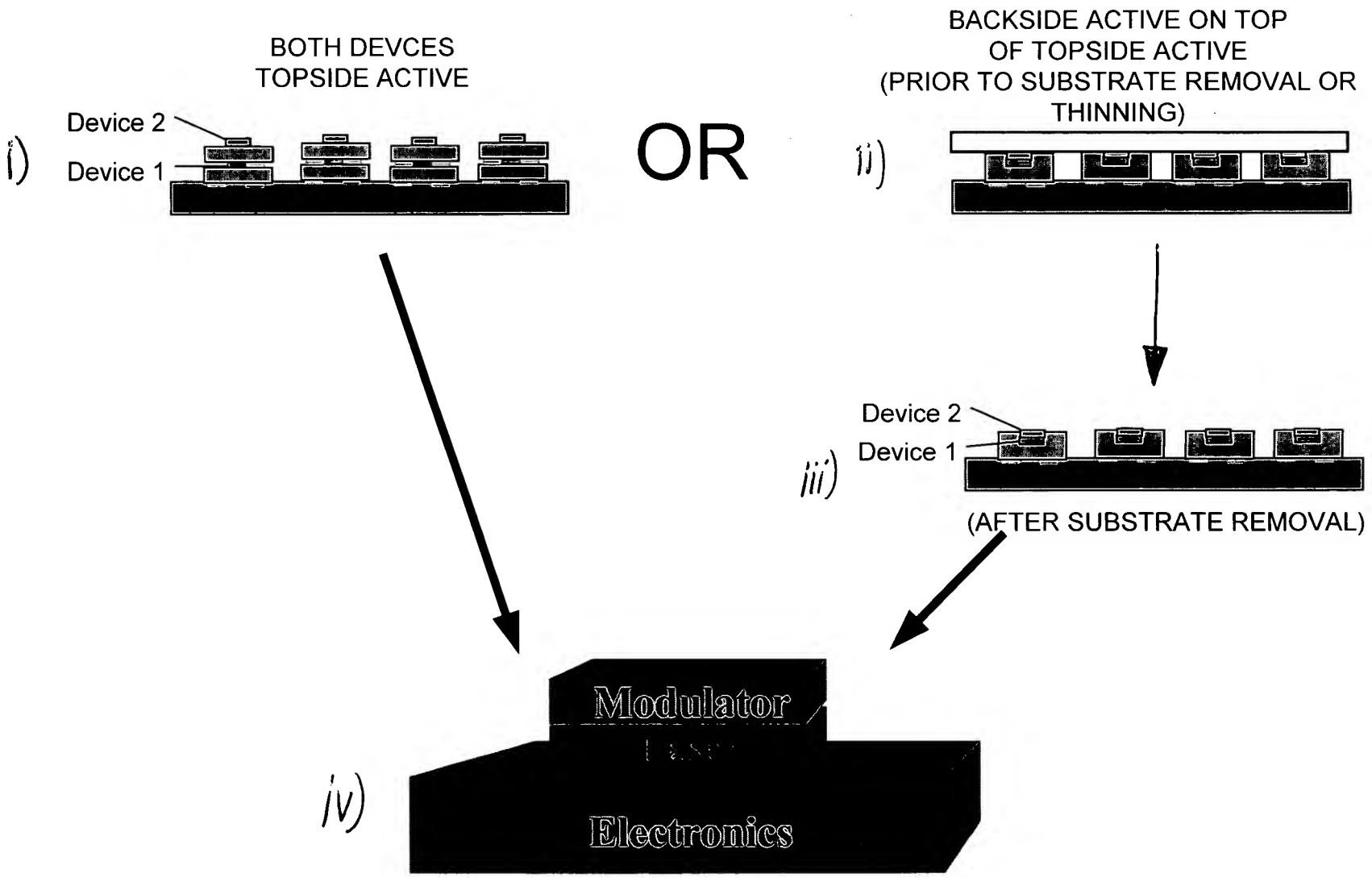


FIG. 20A

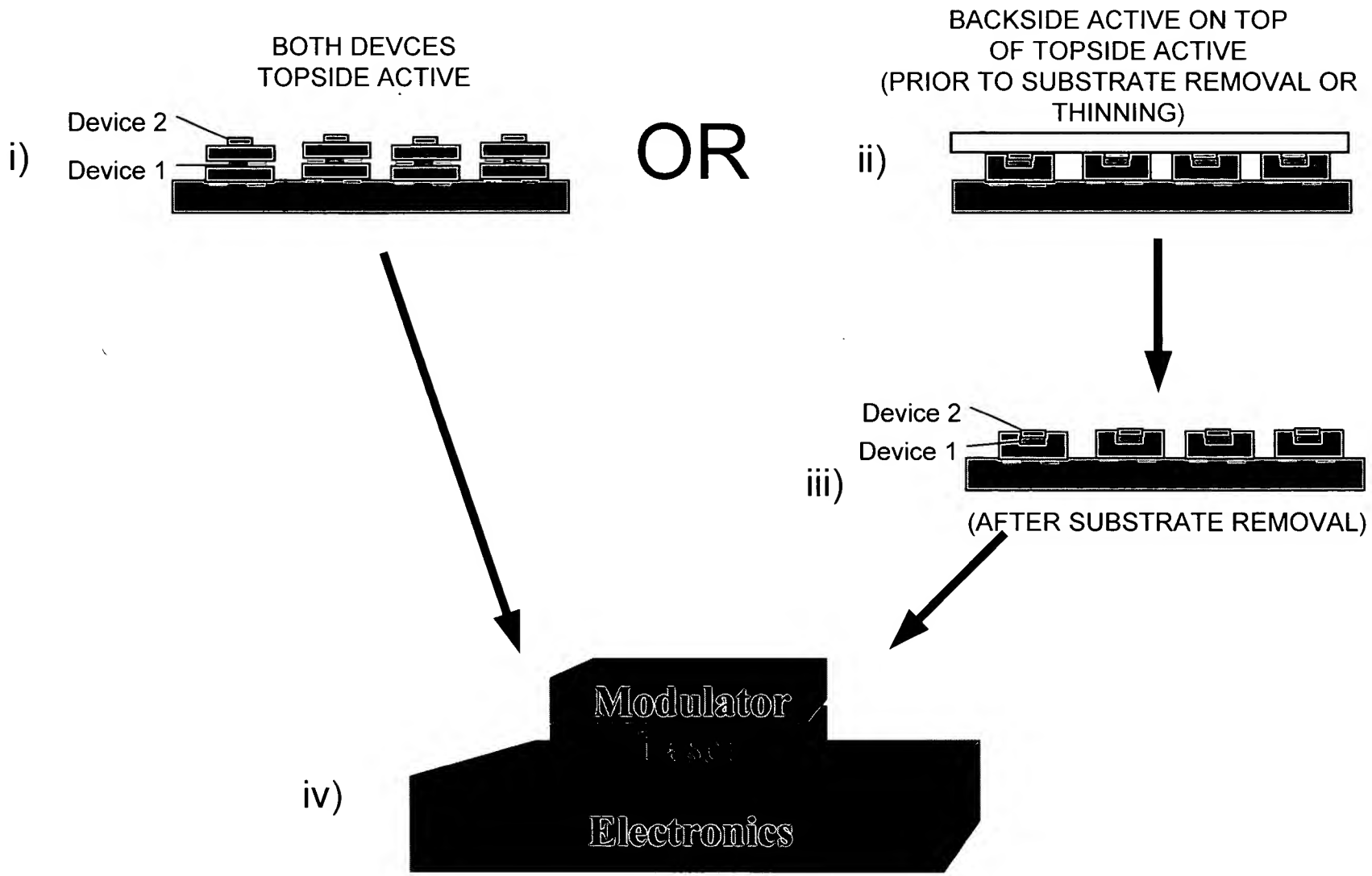


FIG. 20A

40 Gb/s = 20 GHz = 50ps
Wavelength in free space = 3 X 10^{10} cm/s * 50^{12}s = 1.5cm
1/8 wavelength in n=3 = 640 microns

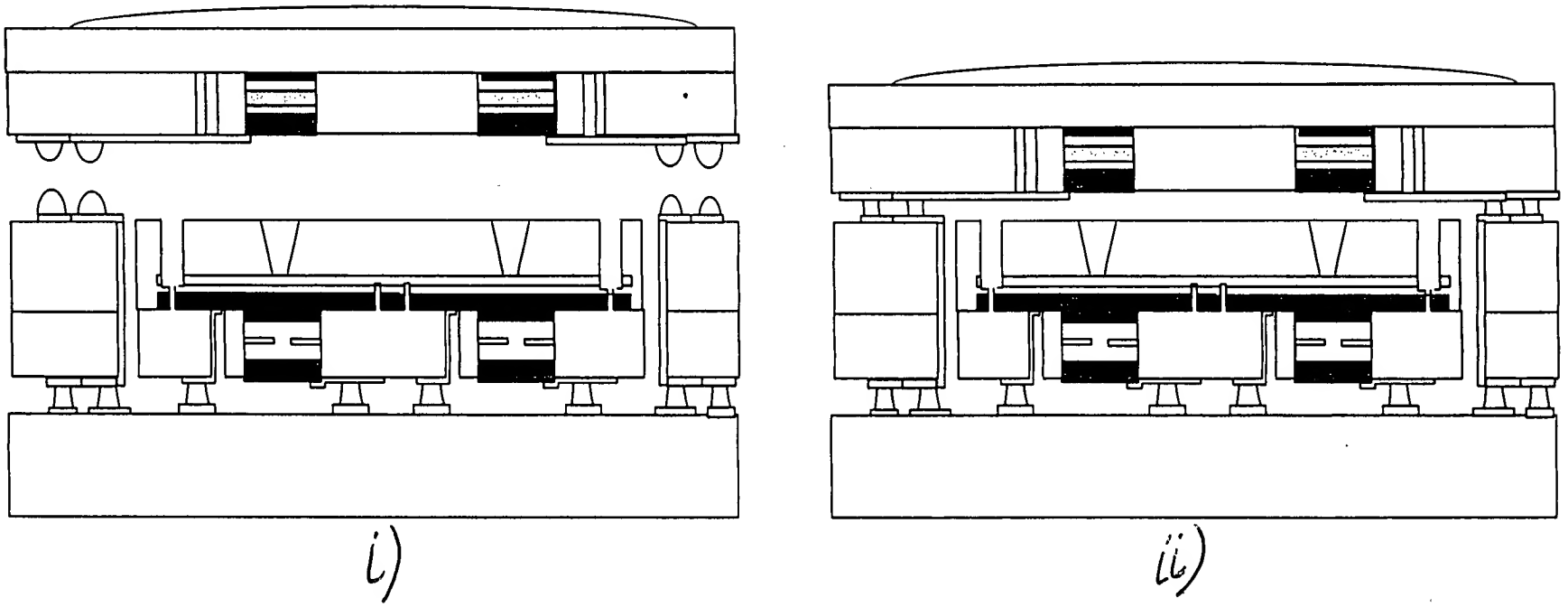
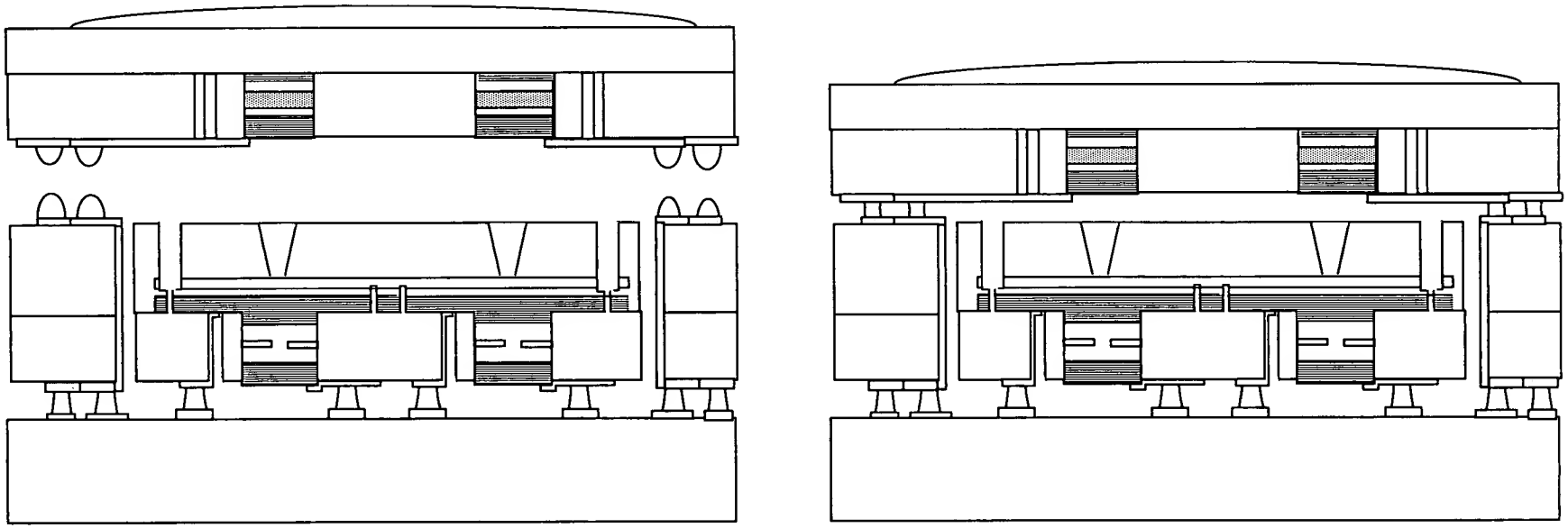


FIG. 20B

40 Gb/s = 20 GHz = 50ps
Wavelength in free space = 3 X 10^{10} cm/s * 50^{12}s = 1.5cm
1/8 wavelength in n=3 = 640 microns



i)

ii)

FIG. 20B

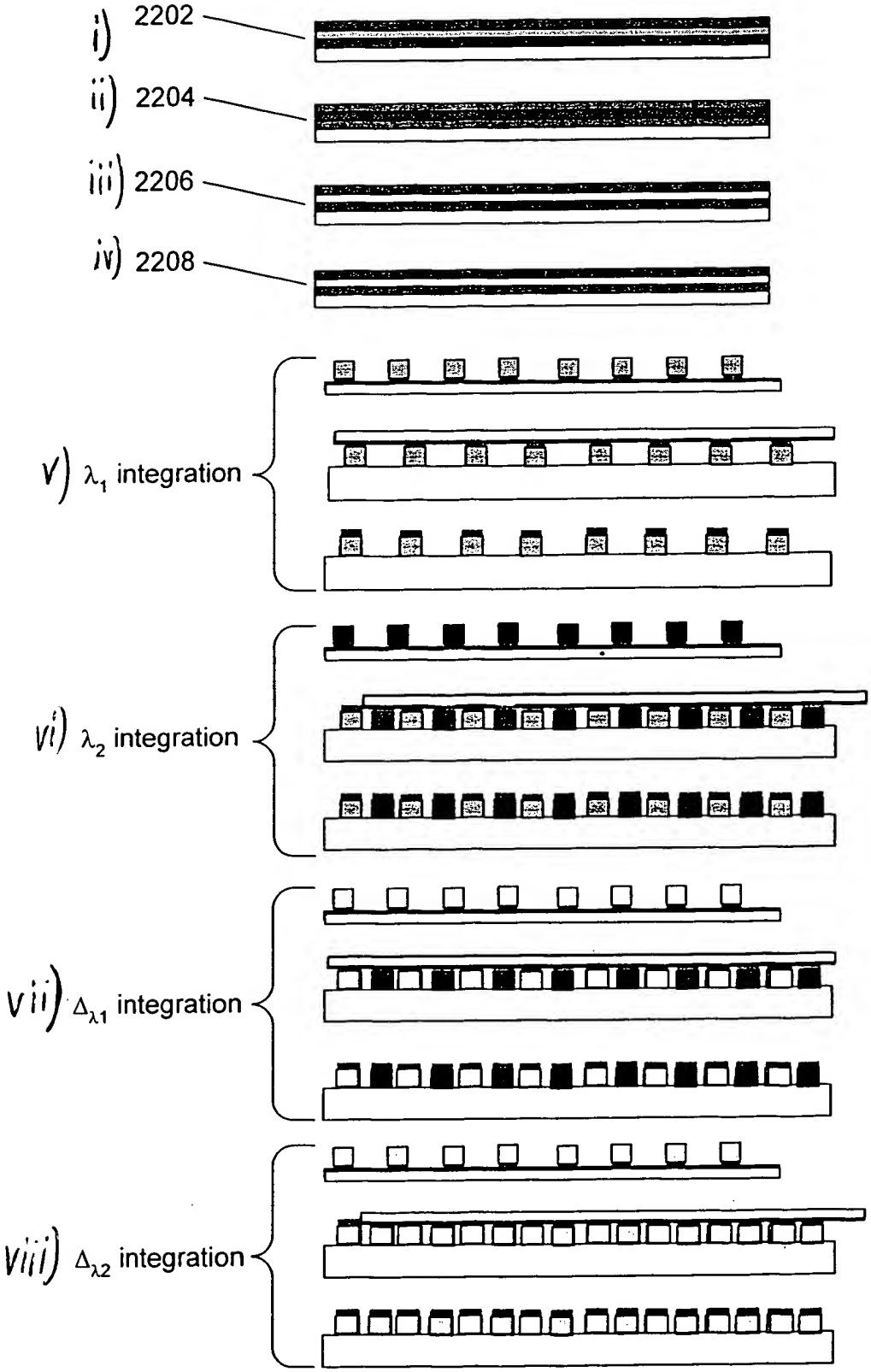


FIG. 22

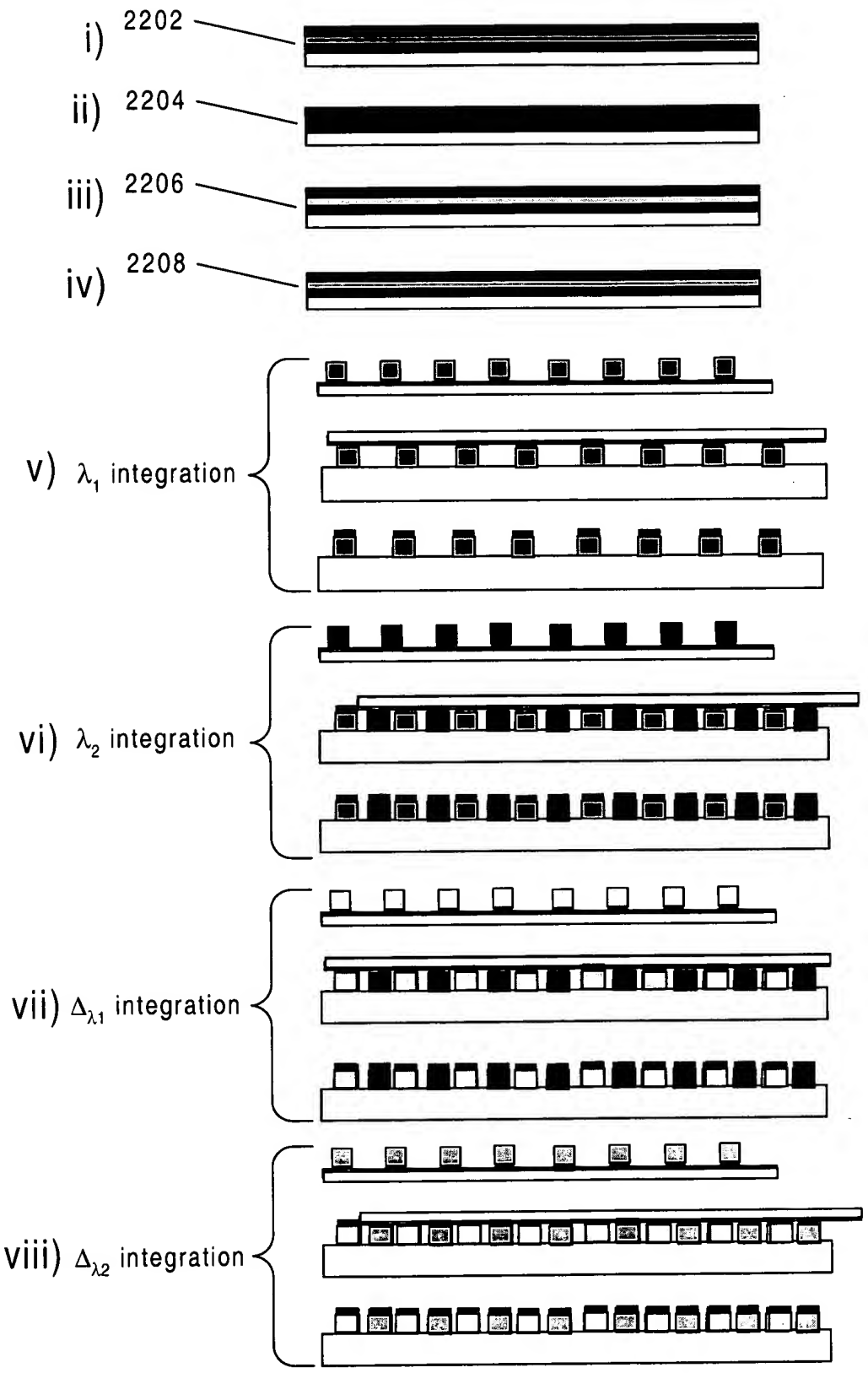
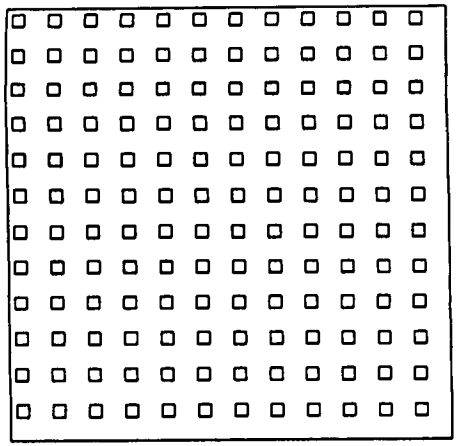
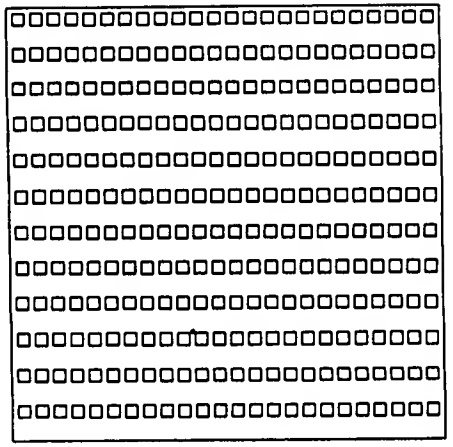


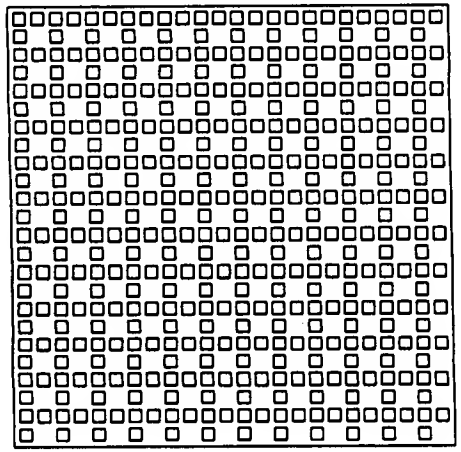
FIG. 22



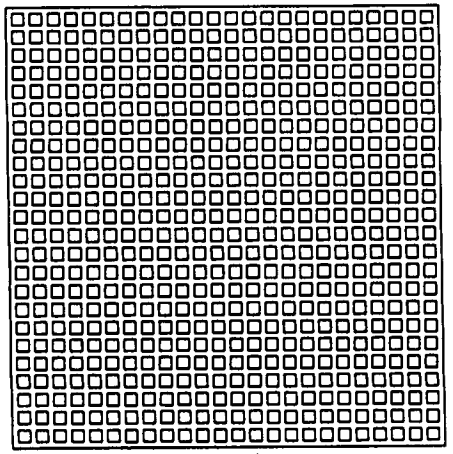
i) λ_1 integration



ii) $\Delta_{\lambda 1}$ integration



iii) λ_2 integration



iv) $\Delta_{\lambda 2}$ integration

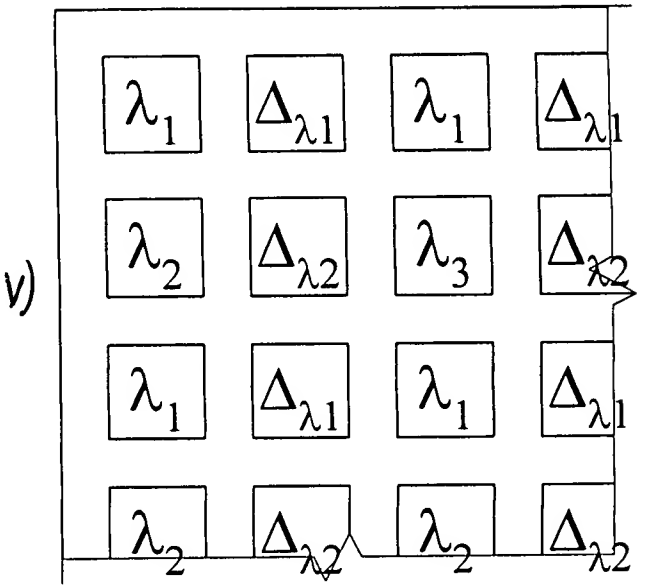
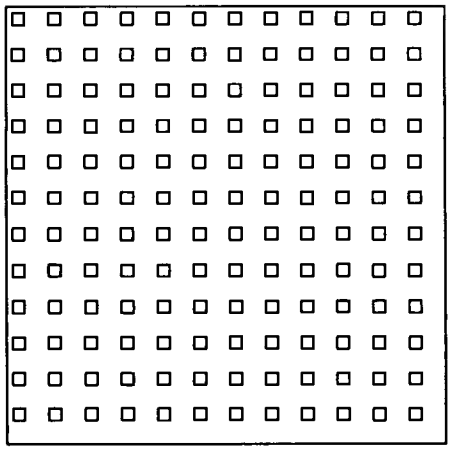
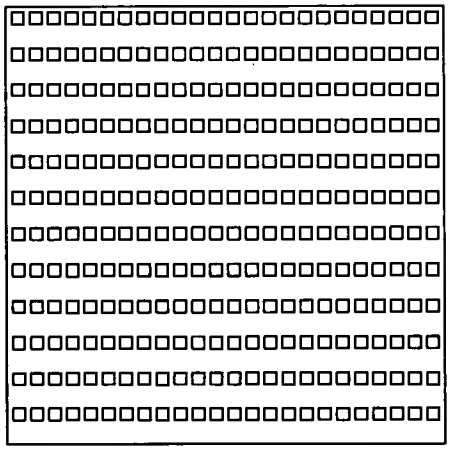


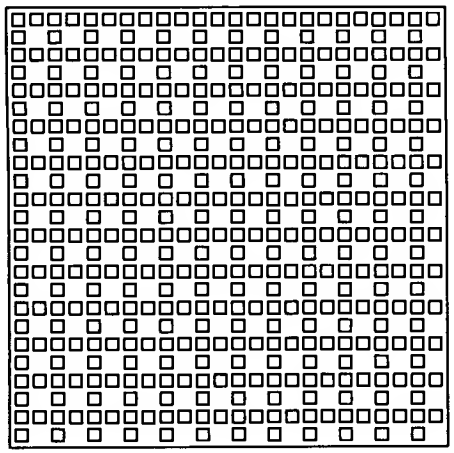
FIG. 23



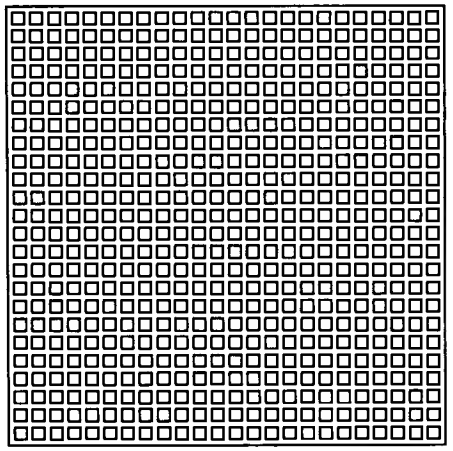
i) λ_1 integration



ii) $\Delta_{\lambda 1}$ integration



iii) λ_2 integration



iv) $\Delta_{\lambda 2}$ integration

v)

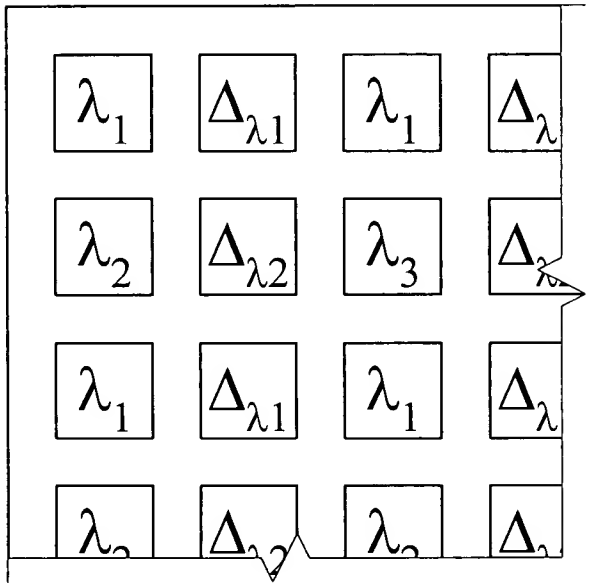


FIG. 23